High-Performance Embedded MCA With USB Interface

eMorpho

The eMorpho is a high-performance multichannel analyzer, designed for use with any kind of scintillator and photomultiplier combination.

Highlights

- **4096 x 32 bit histogram**
- **Very fast: max histogramming rate is 16.5 Mcps**
- **Accurate count rate and anode current measurement**
- **12-bit waveform digitizing ADC**
- **20 MHz to 120 MHz digitization**
- **1024-point waveform capture**
- **340-event list mode buffer**
- **Supports PMT power bases**
- **Purely digital signal processing**
- **Powered through USB interface**
- **Low power: <0.15 W**
- **Data transfer rate: 0.8 Mbyte/s**
- **Small size: 1.25x2-inch PCB**
- **Daisy chain clock and trigger lines**

Photograph of the eMorpho in its desktop housing.

The unit is powered and controlled through its USB interface. The signal can be brought in directly from the photo-multiplier anode into the Detector In BNC input.

Rear connectors support standard and custom GPIO functions, connection to an hvBase (a PMT plug-on high voltage supply and divider). In addition, a JTAG connector makes it possible to reflash the firmware on the device.

The PCB inside is only 1.25x2-inch. It contains the same circuitry as used in the plug-on usbBase, and oemBase.

Specifcations

Features

- The eMorpho is a high-performance embedded multichannel analyzers with extraordinary capabilities. It has been designed for use with any kind of scintillator and photomultiplier combination.
- The 4K by 32-bit histogram offers ample resolution even with the highest resolution scintillators.
- Excellent pileup rejection through built-in pattern recognition.
- Triggered waveform acquisition supports diagnostics and pulse shape analysis studies.
- In list mode the eMorpho stores energies, time stamps and optional pulse shape information.
- Built-in support for pulse shape analysis. One-parameter control achieves neutron/gamma discrimination and supports phoswich detectors.
- Built-in support for embedded PMT high-voltage generators (power bases). See NP and NQ series devices, NP10-0530 and NQ10-0530 in particular.
- Related devices are the eMorpho-LP series for low power applications.

Specifications USB-powered, 12-bit, 40 MHz ADC, unless otherwise noted

Parameter	*Symbol*	*Min*	*Typ.*	*Max*	*Comment*
Interface					
Supply voltage	Vdd	4.35V	5.0V	5.25V	USB standard
External supply voltage	Vdd	3.15V	3.30V	3.45V	If externally powered
Supply current	Idd		60 mA		USB high-power device
Operating temperature range	Top	-40ºC		60ºC	Industrial
Input impedance	Zin		50 Ω		PMT anode signal
MCA function					
Histogram size			4096 x 32 bits		
Minimum time between successive entries	THmin		6 clock cycles		i.e. 150 ns at 40 MHz
Max. periodic update rate	HP_Rate	3.33 Mcps at 20 MHz		16.5 Mcps at 100 MHz	a function of clock speed
Max random pulse update rate	HR_Rate	0.61 Mcps at 20 MHz		3.03 Mcps at 100 MHz	a function of clock speed
MCA readout time	HT_Read	21 ms	32 ms		

Specifications - Continued USB-powered, 10-bit, 20 MHz ADC, unless otherwise noted

Waveform acquisition					
Data size			1024 x 16-bit		
Time between data points	ΔT		1 clock cycle		
Read out time	WT_Read	2.6 ms			dedicated software
List mode operation					
Record length				2048 byte	
Time stamp granularity		50 ns		1 µs	selectable, clock dependent
No. of events per buffer			340		
Buffer readout time	LT_Read	2.6 ms			dedicated software
Analog section					
Input impedance	Zin		50 Ω		
Bandwidth for 60 MHz clock			30 MHz		Due to anti-aliasing filter
Bandwidth for 100 MHz clock			50 MHz		Due to anti-aliasing filter
Gain		101 Ω	102 Ω	103 Ω	100 Ω nominal
		430.0 Ω	431.5 Ω	432.5 Ω	430 Ω nominal
		1099.8 Ω	1101.5 Ω	1103.2 Ω	1100 Ω nominal
		3397.5 Ω	3401.5 Ω	3405.5 Ω	3400 Ω nominal
		10090.5 Ω	10101.5 Ω	10112.5 Ω	10.1 kΩ nominal
ADC input range		1.015 Vpp	1.00 Vpp	1.015 Vpp	

Theory of operation – Overview

The eMorpho-HP is a very compact multichannel analyzer (MCA) and front-end data acquisition system for scintillator detectors with photomultiplier readout.

Its analog section consists of a current to voltage converter with five selectable gains ranging from 100 Ω to 10 kΩ transimpedance. The resulting voltage is presented to a waveform digitizing ADC. Options 20 MHz to 120 MHz sampling rates and a 12-bit, ADC.

A field-programmable gate array (XC6SLX16 FPGA) receives the digitized data stream. It applies all relevant signal processing, performs the histogramming and event storage and communicates with the host computer via a USB-1.2 interface.

The firmware is stored in an on-board EEPROM which boots the FPGA on power up.

Device operation is controlled by just a few commands and parameter settings. Devices settings for more than 20 different scintillator types are provided with the software. The most notable parameters are:

Integration time, IT: Set to match the time over which the scintillator emits most (90%) of its light. For NaI(Tl) IT = 1 μs is most often used. The integration time can be a short as 5 clock cycles or as long as 65535 clock cycles. On a 40 MHz system this corresponds to 150 ns and 1.638 ms.

Trigger threshold: Used to exclude very small signals. Usually set to 1% of the ADC full scale range.

Time to baseline: Used to avoid re-triggering on the noisy tail end of a pulse.

Pile up time: Used by the pile up rejection code. Set to full width at half maximum (fwhm) of the scintillator pulse as seen in the trace display or select from list.

Theory of operation – Signal processing

The digitized waveform reaching the FPGA is an accurate digital image of the incoming signal. The only signal smoothing is caused by an anti-aliasing low pass filter set at half the sampling frequency.

The first step of the signal processing is to measure and remove the DC-offset. After that, pulse heights are determined by computing numerically the integral over the pulse spanning the preset integration time.

As the pulse may be longer than the integration time, the time-to-baseline parameter is used to indicate a wait period during which no measurements of the DC-offset are attempted.

Pile up rejection is achieved by comparing the pulse shape with an expected pattern. In the most simple case, the user provides just the signal width at its half height to achieve excellent pileup rejection.

The trigger system enforces a minimum dead time equal to time-to-baseline at each recognized pulse and extends this when necessary. It keeps an accurate count of real time, accrued dead time, and recognized and rejected pulses to provide a very accurate measurement of the actual incoming pulse count rate.

The firmware is organized into a number of independent modules. Beyond the basic signal processing, these include the communications interface, the control registers, the diagnostics and statistics registers, the histogramming unit, the waveform capture and the list mode unit.

The modular organization makes it possible to easily customize the firmware to user specifications.

Theory of operation – Pulse generator

The firmware includes a pulse generator that can generate single and double pulse with at rates from 1Hz to 1MHz with widths from 1 to 2048 clock cycles and pulse separations of 1 to 256 clock cycles. Its suggested is use is to drive a fast LED such as IF-E92 from Industrial Fiberoptics.

Theory of operation – daisy chains

The eMorpho PCB has 15 general purpose I/O lines that connect directly to the FPGA. This set of 15 signals can be used to interconnect a number of of devices to share clocks, triggers and data. Seven of these signal are available on connector J4.

Multiple eMorphos can be operated in lockstep without suffering from USB command latency through a command chain.

Theory of operation – Software

The eMorpho-HP is delivered with a USB device driver (Windows, DLL) and an application programmer's interface (source code written in C). The device driver is based on libusb (www.libusb.org) and libftdi provided by (http://www.intra2net.com/en/developer/libftdi/

These two driver components exhibit the same API under Windows and Linux, which makes the code portable from desktops down to small embedded systems.

The code is small and has a two-tier hierarchy. There is one I/O function that sends data across the USB cable. All communications with the Morpho are channeled through this I/O function.

The second-tier functions closely reflect the firmware architecture, and for every firmware module there is a corresponding read data function. There are two write data functions, one for each of the two firmware modules that can be written to: the control registers and the user data block RAM.

The control registers contain all parameters that control the Morpho performance.

Wrapper functions simplify the task of setting up the device. For instance, Start_New_Histogram() will set the appropriate bits in the control registers to erase the old histogram and statistics data and begin a new data acquisition.

Finally, when linking to another data acquisition software package it can be advantageous if only one function has to be made available across the interface. Hence, the API includes a wrapper function through which all Morpho commands and data exchanges can be executed.

The eMorpho is intended for OEM applications. Bridgeport Instruments provides a simple GUI (graphics user interface) that demonstrates most of the Morpho functionality. It is written using IGOR PRO from Wavemetrics, and the source code is available to aid developers in their efforts.

Connectors

The two most used connectors are the USB connector (J1) and the BNC input for the PMT anode signal (J2).

J3 – hvBase / Detector

This connector is used to connect to an hvBase. It carries power and controls, the SPI-bus for the temperature sensor on the hvBases and the PMT anode signal.

Pin	*Function*	*Pin*	*Function*
1	GND	2	HV-ctrl
3	T-CLK	4	T-CSB
5	D-CSB	6	T-MISO
7	Vdd for hvBase	8	PMT signal in

Table 1: J3-Pinout. This is an 8-pin connector, type Switchcraft EN3P8.

The hvBase is powered from the eMorpho via the wires on pins 7 and 1. The temperature sensor of the hvBase is read out by the 3 SPI-bus lines T_CLK, T-CSB and T-MOSI. Some firmware versions support a shared SPI bus between the temperature sensor and a high-voltage control DAC on the hvBase. In that case, pin 5 carries the DAC's CSB. Tie to ground when unused.

HV-ctrl is used to set the high voltage of an hvBase when the DAC on the hvBase is not used.

The generated high voltage is HV=1000*HV-ctrl for positive units, and the negative of that for negative-polarity units.

The hvbase returns the PMT anode signal on the wire connected to pin 8, and no BNC cable is needed in that case.

J4 – GPIO

Pin	*Function*	*Pin*	*Function*
1	S0, R_in	2	S1, P_trig_out
3	S4, Seg_in,	4	S3, Pulse_out
5	S6, Seg_out	6	S5, -
7	S2, R_out	8	GND

Table 2: J4-Pinout. This is an 8-pin connector, type Switchcraft EN3P8.

Pins 1, 3, 4, 8are used in the morpho command chain, which allows to operate multiple eMorphos in a coordinated manner, cf the Morpho manual. Pins 2, 4 carry the programmable pulser output (on some firmware versions).

J5– JTAG

Pin	*Function*	*Pin*	*Function*
1	TMS	2	TDO
3	TDI	4	TCK
5	Vref (2.5V)	6	N/C
7	GND	8	N/C

Table 3: J5-Pinout. This is an 8-pin connector, type Switchcraft EN3P8.

Ordering information

Part numbers: eMorpho-ffbb

ff: Sampling rate in MSPS; Use two digits for speeds below 100 MSPS

bb: number of ADC bits (typ. 12 bits).

Examples

12-bit, 80 MSPS, most popular:
eMorpho-2010

12-bit, 120 MSPS, for LaBr3
eMorpho-8012

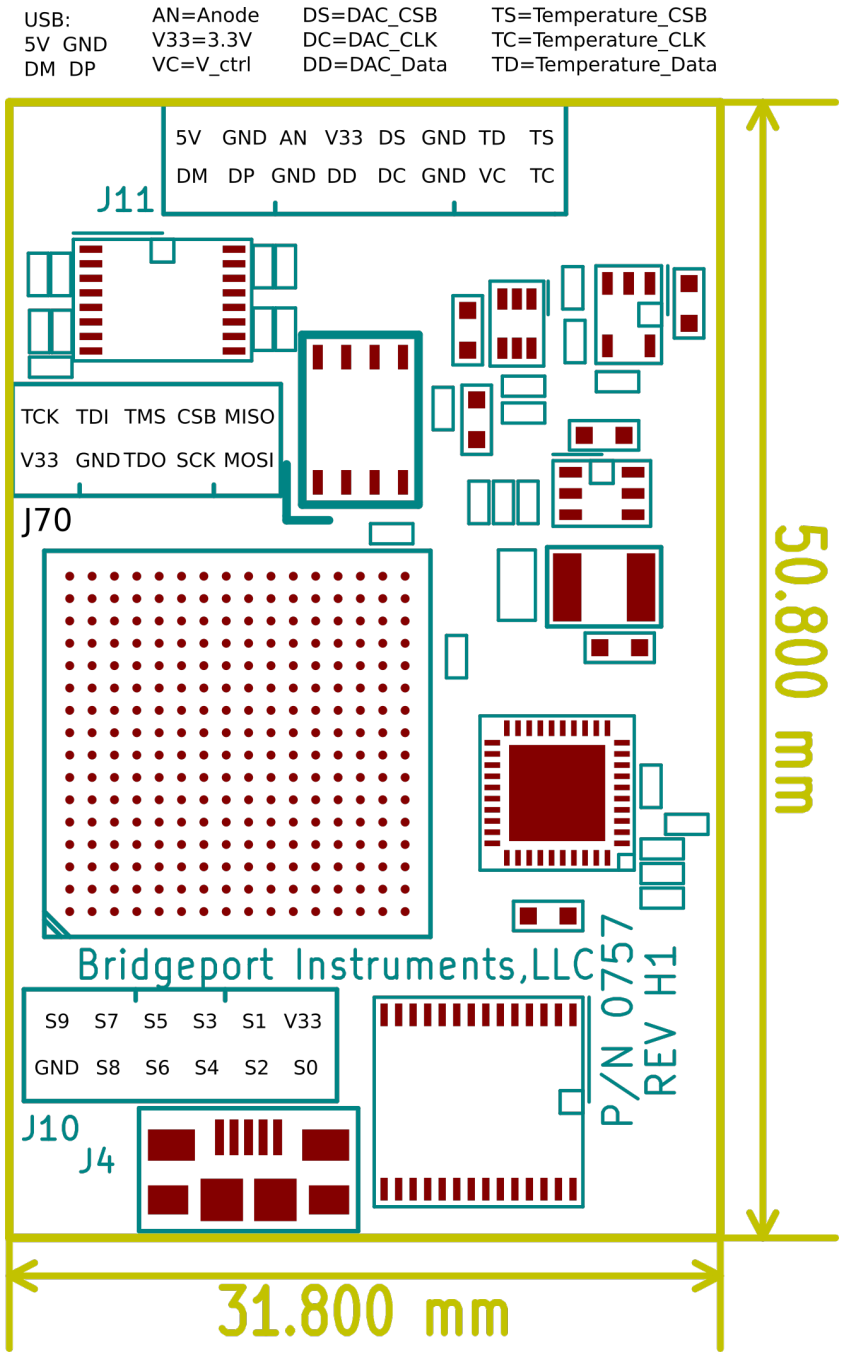

Fig. 1: Position, orientation and pin out of the connectors on the slimMorpho PCB.

J2 is the USB connector, J1 is the JTAG connector for reprogramming the EEPROM from which the FPGA boots. J4 is the GPIO connector and J5 serves the radiation detector.

The view is from the the FPGA side of the PCB onto the PCB.

slimMorpho PCB pinouts – J10

Name	*Description*	*Name*	*Description*	*Name*	*Description*	*Name*	*Description*
S0	R_in	S3	Pulse_out	S6	Seg_out	S9	-
S1	P_Trigger_out	S4	Seg_in	S7	Sus_in	GND	Ground
S2	R_out	S5	-	S8	Sus_out	V33	3.3V_out

Table 4: J10 pinout. All voltage levels are 3.3V CMOS. All Sn-pins can be factory-programmed to implement customer-requested functionality.

slimMorpho PCB pinouts – J11

Name	*Description*	*Name*	*Description*	*Name*	*Description*	*Name*	*Description*
AN	PMT Anode in	DD	HV-DAC data	TD	TC77-Data	5V	USB 5V
GND	Ground	DF	HV-DAC CSB	TF	TC77-CSB	DM	USB D-
V33	3.3V out to HV	DC	HV-DAC CLK	TC	TC77-CLK	DP	USB D+
		Vctrl	HV control			GND	USB GND

Table 5: J11 pinout. All voltage levels are 3.3V CMOS.

Connecting to the PMT:

AN:

PMT anode signal input. DC-coupled, dynamically terminated with 50 Ω. The DC-offset at this input is 0.834V nominal. When using an hvBase, the AN signal is part of that wiring harness.

Connecting to an hvBase:

V33:

Regulated 3.3V supply for an hvBase high voltage unit. Maximum expected draw is 150mA.

HV-control:

Either analog via Vctrl or digital using an SPI interface to the DAC on the hvBase. The three HV-DAC SPI lines are DD, DF, and DC.

Temperature measurement:

There is a temperature sensor (TC77 from microchip.com) on the hvBase. It is read via three SPI lines: TD, TF, and TC.

slimMorpho PCB pinouts – J70

JTAG interface for reprogramming the EEPROM from which the FPGA boots on power up. V33 is the reference voltage and the other 5 JTAG pins carry the same name as the corresponding pins on the Xilinx EEPROM programmer.

The four signals CSB, SCK, MISO and MOSI give direct access to the boot EEPROM.

Connector part numbers and mating parts

Name	*Manufacturer*	*Mfg part no.*	*Mating part*
J1– hvBase	Hirose 12-pin		
J2	BNC (type)	-	-
J3 – USB	Hirose	PX0446 (Buccaneer series)	PX0441(Buccaneer series)
J4 – GPIO	Hirose 12-pin		
J5 – JTAG	Hirose 16-pin		
J70-PCB	Hirose	DF11-10DP-2DSA	DF11-10DP-2C
J10-PCB	Hirose	DF11-12DP-2DSA	DF11-12DP-2C
J11-PCB	Hirose	DF11-16DP-2DSA	DF11-16DP-2C

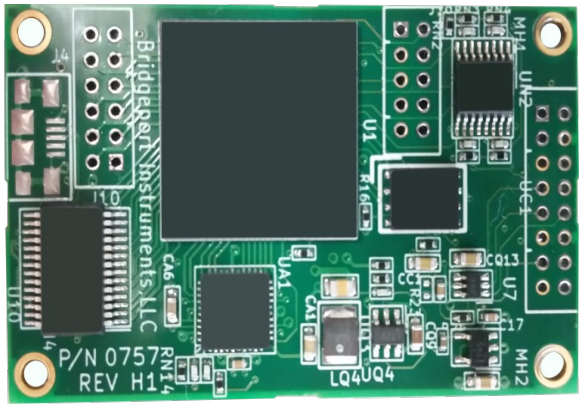

Fig. *2: Photograph of the slimMorpho Rev. H.*

Revision history:

P0	Feb. 2006	Preproduction release, initial document
P1	Feb. 2006	Preproduction release, updated connector description for eMorpho-HPS
P2	Feb. 2006	Preproduction release, updated ordering information
P3	Mar. 2006	Preproduction release, added 12-bit 20MHz version
P4	Sep. 2006	Last preproduction release; updated ordering information
R1	Oct. 2006	Production release
R2	Jan. 2009	Updated ordering information
R6	Nov. 2011	Updated ordering information, housing description and connector pin-outs
R7	Feb. 2014	Updated connector pin-outs to using slimMorpho
R8	Dec. 2017	Updated to new, lower, power consumption; new connector pinouts.